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Jameco Part Number 235299



FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

# 74AC175 • 74ACT175
# Quad D-Type Flip-Flop

## General Description

The AC/ACT175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D-type inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D-type inputs, when LOW.

## Features

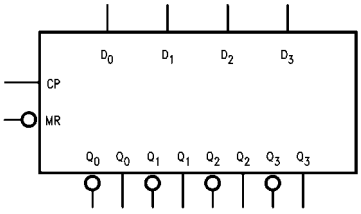
- $I_{CC}$ reduced by 50%
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24 mA
- ACT175 has TTL-compatible inputs

## Ordering Code:

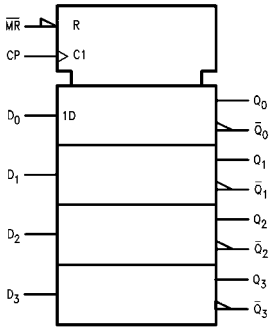
| Order Number | Package Number | Package Description |
|---|---|---|
| 74AC175SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74AC175SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC175MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC175PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT175SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74ACT175SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT175MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT175PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

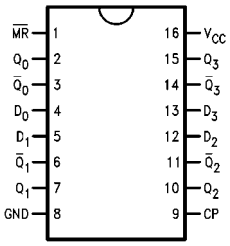
## Logic Symbols




**IEEE/IEC**




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_3$ | Data Inputs |
| CP | Clock Pulse Input |
| $\overline{MR}$ | Master Reset Input |
| $Q_0$–$Q_3$ | True Outputs |
| $\overline{Q}_0$–$\overline{Q}_3$ | Complement Outputs |

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## Functional Description

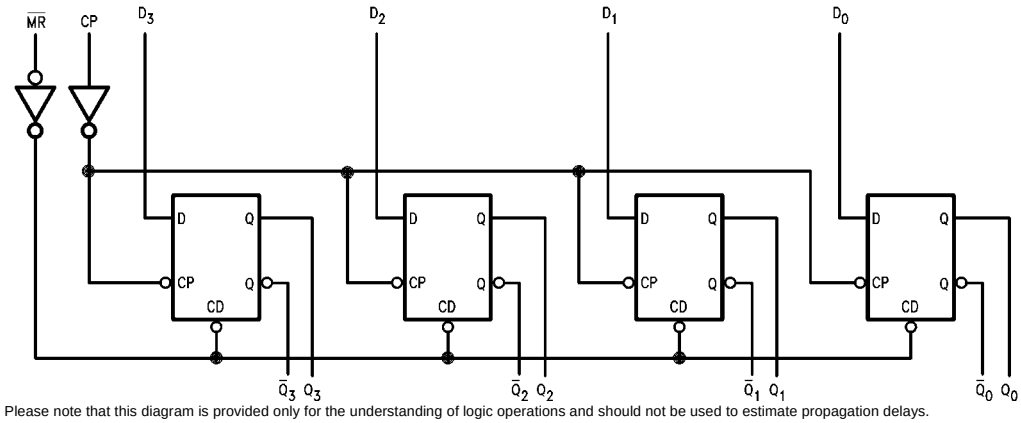
The AC/ACT175 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The AC/ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

## Truth Table

| Inputs | Outputs | |
|---|---|---|
| @ $t_n$, $\overline{MR}$ = H | @ $t_{n+1}$ | |
| $D_n$ | $Q_n$ | $\overline{Q}_n$ |
| L | L | H |
| H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
$t_n$ = Bit Time before Clock Pulse
$t_{n+1}$ = Bit Time after Clock Pulse

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source | |
| or Sink Current ($I_O$) | ± 50 mA |
| DC $V_{CC}$ or Ground Current | |
| per Output Pin ($I_{CC}$ or $I_{GND}$) | ± 50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| AC | 2.0V to 6.0V |
| ACT | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | |
| AC Devices | |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate (ΔV/Δt) | |
| ACT Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications

## DC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C Typ | $T_A$ = −40°C to +85°C Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level | 3.0 | 1.5 | 2.1 | 2.1 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 3.15 | 3.15 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | |
| $V_{IL}$ | Maximum LOW Level | 3.0 | 1.5 | 0.9 | 0.9 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 1.35 | 1.35 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | |
| $V_{OH}$ | Minimum HIGH Level | 3.0 | 2.99 | 2.9 | 2.9 | | |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 2.56 | 2.46 | | $I_{OH}$ = −12 mA |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA (Note 2) |
| $V_{OL}$ | Maximum LOW Level | 3.0 | 0.002 | 0.1 | 0.1 | | |
| | Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 0.36 | 0.44 | | $I_{OL}$ = 12 mA |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 2) |
| $I_{IN}$ (Note 4) | Maximum Input Leakage Current | 5.5 | | ±0.1 | ± 1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 3) | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ (Note 4) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

## DC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ | $T_A = -40°C$ to $+85°C$ | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum HIGH Level | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ |
| | Input Voltage | 5.5 | 1.5 | 2.0 | 2.0 | | or $V_{CC} - 0.1V$ |
| $V_{IL}$ | Maximum LOW Level | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ |
| | Input Voltage | 5.5 | 1.5 | 0.8 | 0.8 | | or $V_{CC} - 0.1V$ |
| $V_{OH}$ | Minimum HIGH Level | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50\ \mu A$ |
| | Output Voltage | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN} = V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH} = -24$ mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH} = -24$ mA (Note 5) |
| $V_{OL}$ | Maximum LOW Level | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50\ \mu A$ |
| | Output Voltage | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN} = V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL} = 24$ mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL} = 24$ mA (Note 5) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ± 1.0 | μA | $V_I = V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max |
| $I_{OHD}$ | Output Current(Note 6) | 5.5 | | | −75 | mA | $V_{OHD} = 3.85V$ Min |
| $I_{CC}$ | Maximum Quiescent | 5.5 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ |
| | Supply Current | | | | | | or GND |

**Note 5:** All outputs loaded; thresholds on input associated with output under test.

**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | (Note 7) | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock | 3.3 | 149 | 214 | | 139 | | MHz |
| | Frequency | 5.0 | 187 | 244 | | 187 | | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 2.0 | 9.5 | 12.0 | 2.0 | 13.5 | ns |
| | CP to $Q_n$ or $\overline{Q}_n$ | 5.0 | 1.5 | 7.0 | 9.0 | 1.0 | 9.5 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 2.5 | 8.5 | 13.0 | 2.0 | 14.5 | ns |
| | CP to $Q_n$ or $\overline{Q}_n$ | 5.0 | 1.5 | 6.0 | 9.5 | 1.5 | 10.5 | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 3.0 | 7.5 | 12.5 | 2.5 | 13.5 | ns |
| | $\overline{MR}$ to $\overline{Q}_n$ | 5.0 | 2.0 | 5.5 | 9.0 | 1.5 | 10.0 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 3.0 | 8.5 | 11.0 | 2.5 | 12.5 | ns |
| | $\overline{MR}$ to $Q_n$ | 5.0 | 2.0 | 6.0 | 8.5 | 1.5 | 9.0 | |

**Note 7:** Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements for AC

| Symbol | Parameter | $V_{CC}$ (V) (Note 8) | $T_A = +25°C$, $C_L = 50$ pF | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW | 3.3 | 2.0 | 4.5 | 4.5 | ns |
| | $D_n$ to CP | 5.0 | 1.0 | 3.0 | 3.0 | |
| $t_H$ | Hold Time, HIGH or LOW | 3.3 | 1.0 | 1.0 | 1.0 | ns |
| | $D_n$ to CP | 5.0 | 1.0 | 1.0 | 1.0 | |
| $t_W$ | CP Pulse Width | 3.3 | 2.5 | 4.5 | 4.5 | ns |
| | HIGH or LOW | 5.0 | 2.0 | 3.5 | 3.5 | |
| $t_W$ | $\overline{MR}$ Pulse Width, LOW | 3.3 | 2.5 | 4.5 | 5.0 | ns |
| | | 5.0 | 2.0 | 3.5 | 3.5 | |
| $t_{REC}$ | Recovery Time | 3.3 | −2.0 | 0 | 0 | ns |
| | $\overline{MR}$ to CP | 5.0 | −1.0 | 0 | 0 | |

**Note 8:** Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) (Note 9) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | 5.0 | 175 | 236 | | 145 | | MHz |
| $t_{PLH}$ | Propagation Delay CP to $Q_n$ or $\overline{Q}_n$ | 5.0 | 2.0 | 6.0 | 10.0 | 1.5 | 11.0 | ns |
| $t_{PHL}$ | Propagation Delay CP to $Q_n$ or $\overline{Q}_n$ | 5.0 | 2.0 | 7.0 | 11.0 | 1.5 | 12.0 | ns |
| $t_{PLH}$ | Propagation Delay $\overline{MR}$ to $\overline{Q}_n$ | 5.0 | 2.0 | 6.0 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $Q_n$ | 5.0 | 2.0 | 5.5 | 9.5 | 1.5 | 10.5 | ns |

**Note 9:** Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements for ACT

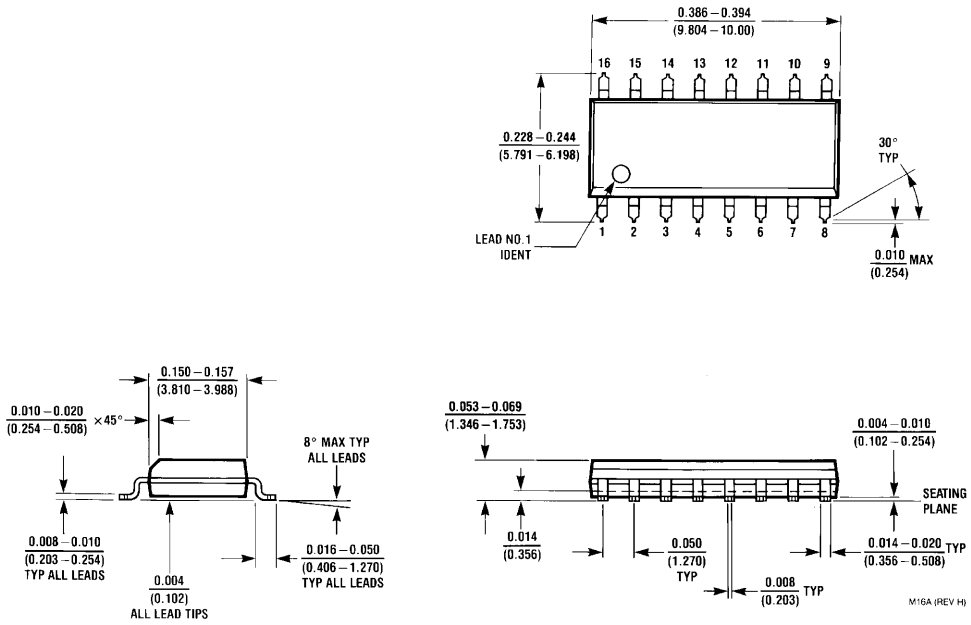
| Symbol | Parameter | $V_{CC}$ (V) (Note 10) | $T_A = +25°C$, $C_L = 50$ pF | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ (H) | Setup Time | 5.0 | 3.0 | 2.0 | 2.0 | ns |
| $t_S$ (L) | $D_n$ to CP | | 3.0 | 2.5 | 2.5 | |
| $t_H$ | Hold Time, HIGH or LOW $D_n$ to CP | 5.0 | 0 | 1.0 | 1.0 | ns |
| $t_W$ | CP Pulse Width HIGH or LOW | 5.0 | 4.0 | 3.0 | 3.5 | ns |
| $t_W$ | $\overline{MR}$ Pulse Width, LOW | 5.0 | 4.0 | 3.0 | 4.0 | ns |
| $t_{rec}$ | Recovery Time, $\overline{MR}$ to CP | 5.0 | 0 | 0 | 0 | ns |

**Note 10:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

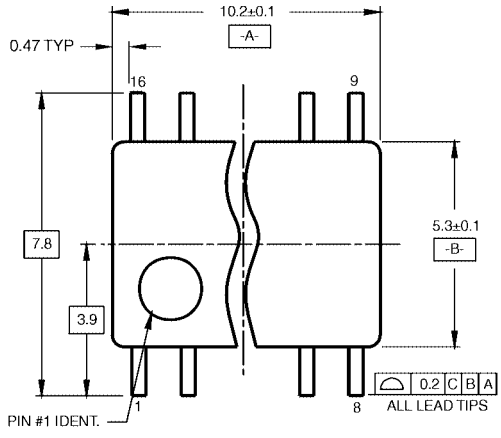
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 45.0 | pF | $V_{CC}$ = 5.0V |

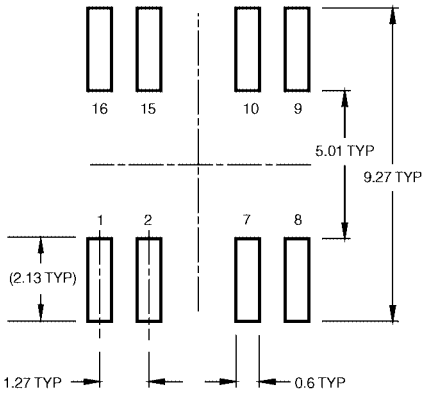
## Physical Dimensions inches (millimeters) unless otherwise noted



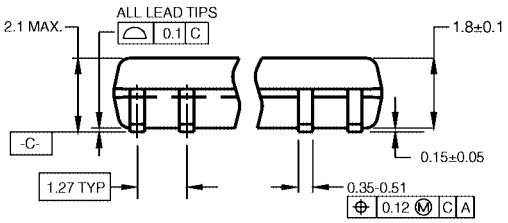

**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow Body**
**Package Number M16A**

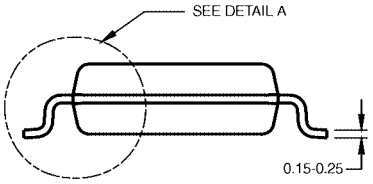
## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



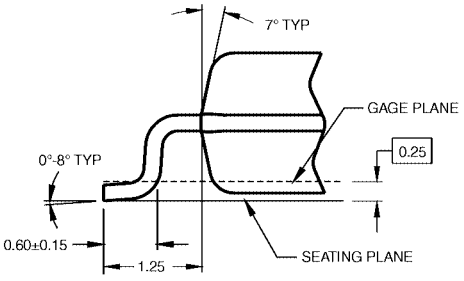




LAND PATTERN RECOMMENDATION




DIMENSIONS ARE IN MILLIMETERS




DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

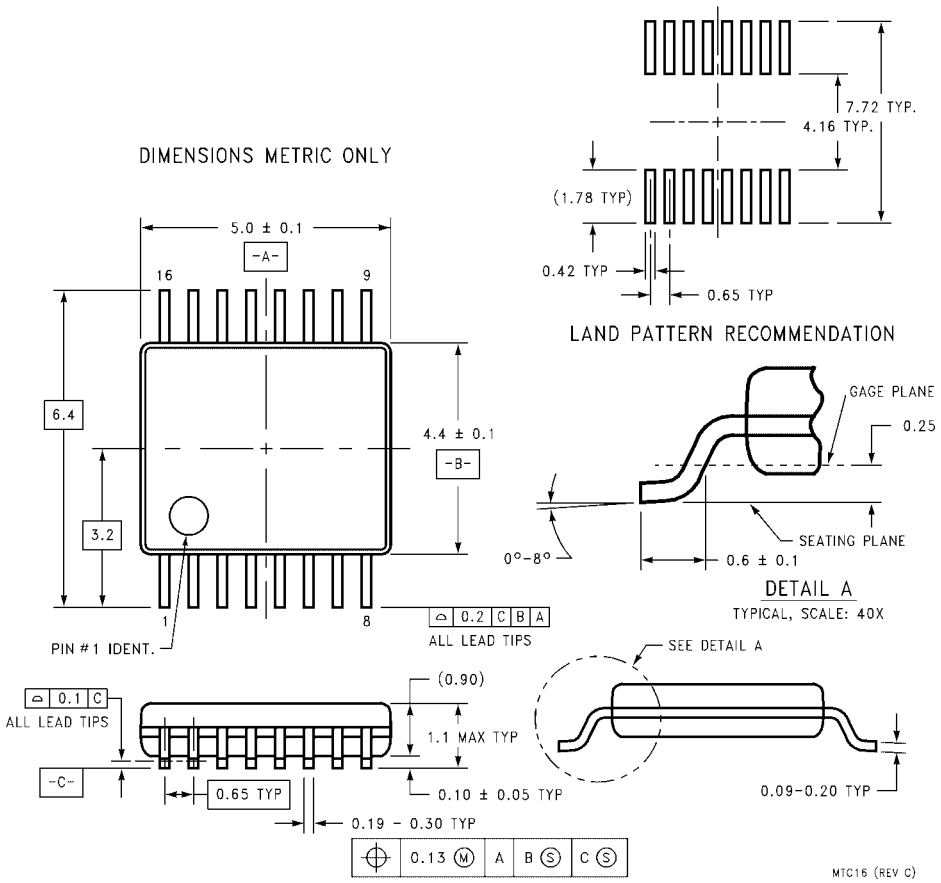
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

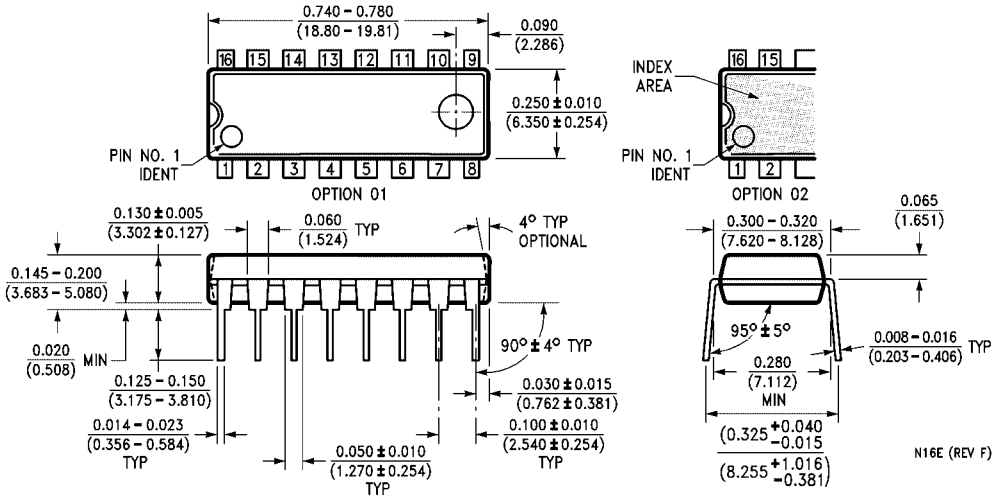
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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